IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Douglas T. Haydeen	Examiner: Ryan M. Stiglic
Serial No.:	10/759,819	Group Art Unit: 2112
Filed:	January 16, 2004	Docket No.: 10002614-1
Title:	Bus Device Insertion and Removal System	

APPEAL BRIEF UNDER 37 C.F.R. § 41.37

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal Brief is filed in response to the Final Office Action mailed September 14, 2006 and Notice of Appeal filed on November 30, 2007.

AUTHORIZATION TO DEBIT ACCOUNT

It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's deposit account no. 08-2025.

I. REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP, a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences known to appellant, the appellant's legal representative, or assignee that will directly affect or be directly affected by or have a bearing on the Appeal Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1 – 7, 9 – 11, and 31 – 36 stand finally rejected. Claims 8 and 12-30 are canceled. The rejection of claims 1 – 7, 9 – 11, and 31 – 36 is appealed.

IV. STATUS OF AMENDMENTS

No amendments were made after receipt of the Final Office Action. All amendments have been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following provides a concise explanation of the subject matter defined in each of the claims involved in the appeal, referring to the specification by page and line number and to the drawings by reference characters, as required by 37 C.F.R. § 41.37(c)(1)(v). Each element of the claims is identified by a corresponding reference to the specification and drawings where applicable. Note that the citation to passages in the specification and drawings for each claim element does not imply that the limitations from the specification and drawings should be read into the corresponding claim element or that these are the sole sources in the specification supporting the claim features.

Paragraph [0005] in Applicant's specification provides a summary as follows: In one embodiment, the system comprises a bus comprising signal lines and a device configured to be inserted onto and removed from the bus through contacts. The contacts are configured to provide at different times during insertion and removal contact between a pre-charge circuit and one of the signal lines, and a low-impedance across the pre-charge circuit.

Further, support for the independent claims appears as follows:

Claim 1

A system (FIGS. 1-6: #20) comprising:

a bus (#24) comprising signal lines (#46, #48: paragraphs [0025], [0026]); and

a device (#26) configured to be inserted onto and removed from the bus through contacts (#40) configured to provide at different times during insertion and removal contact between a pre-charge circuit and one of the signal lines, and a low-impedance across the pre-charge circuit (paragraphs [0016], [0027 – 0035]).

Claim 31

A system (FIGS. 1-6: #20), comprising:

a bus (#24) comprising signal lines (#46, #48: paragraphs [0025], [0026]);

a device (#26) configured to be inserted onto and removed from the bus through contacts configured to provide at different times during insertion and removal contact between a pre-charge circuit and one of the signal lines, and a low-impedance across the pre-charge circuit (paragraphs [0016], [0027 – 0035]),

the contacts comprising a connector system (#40) including a first connector (#64), a second connector (#80), where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line, and the second connector is configured to provide a first short-circuit between the second connector and the first bus signal line, where the first connector and the second connector are staggered to provide the first pre-charge circuit and the first short-circuit at different times during engagement and disengagement of the connector system (paragraphs [0016], [0027 – 0035]).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-6, 9-10, 31-33, and 35 are rejected under 35 USC § 103(a) as being unpatentable over USPN 5,729,062 (Satoh).

Claim 7 is rejected under 35 USC § 103(a) as being unpatentable over USPN 5,729,062 (Satoh) in view of Paul Li.

Claim 11 is rejected under 35 USC § 103(a) as being unpatentable over USPN 5,729,062 (Satoh) in view of The I2C Specification.

Claims 34 and 36 are rejected under 35 USC § 103(a) as being unpatentable over USPN 5,729,062 (Satoh) in view of USPN 5,644,731 (Liencres).

VII. ARGUMENT

The rejection of claims 1 – 7, 9 – 11, and 31 – 36 is improper, and Applicant respectfully requests withdraw of these rejections.

The claims do not stand or fall together. Instead, Applicant presents separate arguments for the independent claims. Each of these arguments is separately argued below and presented with separate headings and sub-heading as required by 37 C.F.R. § 41.37(c)(1)(vii).

Claim Rejections: 35 USC § 103(a)

Claims 1-6, 9-10, 31-33, and 35 are rejected under 35 USC § 103(a) as being unpatentable over USPN 5,729,062 (Satoh). These rejections are traversed.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143. For at least the following reasons, Applicant asserts that the rejection does not satisfy these criteria.

Overview of Satoh

The Satoh Patent is directed to an active plug-in circuit that includes a mode setting section that sets either a plug-in mode or a regular mode depending on the power source voltage of the package. When the plug-in mode is set, a power consumption controller maintains an electronic circuit built in the package in a low power consumption mode. After the power source voltage of the electronic circuit has been stabilized, the mode setting section sets the regular mode. The active plug-in circuit is capable of reducing the variation of a power source current occurring when the power source pin of a package connector is connected to the corresponding terminal of a mother board connector and during the transition from a plug-in mode to a regular mode.

Claim 1

Satoh does not teach or suggest all of the elements recited in independent claim 1. Examples for this claim are provided below.

As a first example, claim 1 recites a device inserted and removed from a bus "through contacts configured to provide **at different times** during insertion and removal **between a pre-charge circuit and one of the signal lines**" (emphasis added). In other words, when the device is being inserted to or removed from the bus, contacts between a pre-charge circuit and a signal line engage at different times.

The Examiner argues that these elements are taught in Fig. 5 of Satoh. Applicants respectfully disagree. Fig. 5 in Satoh shows a configuration for establishing a low power consumption mode in circuit 14. Two switches 15a, 15b are open from a plug-in mode signal output to the mode signal line 13. Notice that nowhere does Satoh teach or suggest that contacts between a pre-charge circuit and a signal line engage at different times. Where is the pre-charge circuit in Fig. 5 of Satoh? Where are the "contacts" that engage "at different times?" Such elements are not suggested in Satoh.

For at least these reasons, independent claim 1 and its respective dependent claims are allowable over Satoh.

As a second example, claim 1 recites a low-impedance across the pre-charge circuit. Satoh does discuss a low power consumption mode in connection with Fig. 5 (see col. 4, lines 38-39), but nowhere does Satoh suggest "a low-impedance across the pre-charge circuit." The concept of a low power consumption mode and the concept of low-impedance across the pre-charge circuit are quite different. No suggestion whatsoever exists in Satoh for providing a low-impedance across a pre-charge circuit.

For at least these reasons, independent claim 1 and its respective dependent claims are allowable over Satoh.

As a third example, the Examiner admits the following: "Satoh does not expressly disclose such a pre-charge circuit and a low-impedance short circuit on the bus signal lines 15a and 15b of figure 5" (see Final OA at p. 4). Applicants agree with this admission. The Examiner, however, attempts to cure this glaring deficiency with a generalization on obviousness:

> Satoh however admits, "Various modifications will become possible for those skilled in the art after receiving the teachings of the present disclosure without departing from the scope thereof (col. 7, ll. 1-3)" (see Final OA at p. 4).

Applicants respectfully assert that a generalization on various modifications in Satoh is not sufficient to suggest to one skilled in art a specific embodiment (i.e., the embodiment recited in the claims). The Examiner has provided no explanation whatsoever as to explain why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification based merely on a generalization in Satoh.

For at least these reasons, independent claim 1 and its respective dependent claims are allowable over Satoh.

Claim 31

Satoh does not teach or suggest all of the elements recited in independent claim 31. Examples for this claim are provided below.

As a first example, claim 31 recites a device inserted and removed from a bus "through contacts configured to provide **at different times** during insertion and removal **between a pre-charge circuit and one of the signal lines**" (emphasis added). This recitation is similar to the recitation argued in connection with claim 1. Thus for at least the respective reasons provided above, claim 31 and its dependent claims are allowable over Satoh.

As a second example, claim 31 recites a low-impedance across the pre-charge circuit. This recitation is similar to the recitation argued in connection with claim 1. Thus for at least the respective reasons provided above, claim 31 and its dependent claims are allowable over Satoh.

As a third example, the Examiner admits the following: "Satoh does not expressly disclose such a pre-charge circuit and a low-impedance short circuit on the bus signal lines 15a and 15b of figure 5" (see Final OA at p. 4). Applicant addressed this argument

above in connection with claim 1. Thus for at least the respective reasons provided above, claim 31 and its dependent claims are allowable over Satoh.

As a fourth example, claim 31 recites a connector system including a first connector and a second connector, where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line. Where are these two connectors in Satoh? In other words, where does Satoh teach or suggest two connectors where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line? Such teachings or suggestions do not exist. Satoh never suggests to modify the clock terminal or the data terminal in his figures to include any circuitry attached to the power supply contacts.

The Examiner argues that the claimed connectors are shown at #59 and #57 in Fig. 9 of Satoh. Applicants respectfully disagree. Numbers 57 and 59 are connectors, but connector 57 is not configured to provide a pre-charge circuit between connector 59 and a bus signal line. This arrangement simply does not exist in Fig. 9. By contrast, Fig. 9 shows a power consumption controller 53 that maintains the circuit 52 in low power consumption until a regular mode signal is provided (see col. 6, lines 14-17). No pre-charge circuit exists.

For at least these reasons, claim 31 and its dependent claims are allowable over Satoh.

As a fifth example, claim 31 recites the second connector is configured to provide a first short-circuit between the second connector and the first bus signal line. Satoh does not teach or suggest this arrangement of elements. The Examiner cites col. 5, line 62 – col. 6, line 27 in Satoh. This section of Satoh discusses Fig. 9. Where is a second conductor that provides a short-circuit between itself and a bus line? This arrangement is not show or suggested in Fig. 9 of Satoh.

For at least these reasons, claim 31 and its dependent claims are allowable over Satoh.

As a sixth example, claim 31 recites where the first connector and the second connector are staggered to provide the first pre-charge circuit and the first short-circuit at different times during engagement and disengagement of the connector system. In contrast, Satoh is directed to power supply contacts and reducing the variation of a power

source current occurring when the power source pin of a package connector is connected to the corresponding terminal of a mother board connector and during the transition from a plug-in mode to a regular mode.

For at least these reasons, claim 31 and its dependent claims are allowable over Satoh.

Claim Rejections: 35 USC § 103(a)

Claim 7 is rejected under 35 USC § 103(a) as being unpatentable over USPN 5,729,062 (Satoh) in view of Paul Li. Claim 7 depends from claim 1. As noted above, Satoh fails to teach or suggest all the elements of claim 1. Paul Li fails to cure these deficiencies. Thus, for at least the reasons provided with respect to independent claim 1, dependent claim 7 is allowable over Satoh and Paul Li.

Claim Rejections: 35 USC § 103(a)

Claim 11 is rejected under 35 USC § 103(a) as being unpatentable over USPN 5,729,062 (Satoh) in view of The I2C Specification. Claim 11 depends from claim 1. As noted above, Satoh fails to teach or suggest all the elements of claim 1. The I2C Specification fails to cure these deficiencies. Thus, for at least the reasons provided with respect to independent claim 1, dependent claim 11 is allowable over Satoh and The I2C Specification.

Claim Rejections: 35 USC § 103(a)

Claims 34 and 36 are rejected under 35 USC § 103(a) as being unpatentable over USPN 5,729,062 (Satoh) in view of USPN 5,644,731 (Liencres). Claims 34 and 36 depend from claim 31. As noted above, Satoh fails to teach or suggest all the elements of claim 31. Liencres fails to cure these deficiencies. Thus, for at least the reasons provided with respect to independent claim 31, dependent claims 34 and 36 are allowable over Satoh and Liencres.

CONCLUSION

In view of the above, Applicant respectfully requests the Board of Appeals to reverse the Examiner's rejection of all pending claims.

Any inquiry regarding this Amendment and Response should be directed to Philip S. Lyren at Telephone No. 832-236-5529. In addition, all correspondence should continue to be directed to the following address:

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VIII. Claims Appendix

1. A system comprising:

a bus comprising signal lines; and

a device configured to be inserted onto and removed from the bus through contacts configured to provide at different times during insertion and removal contact between a pre-charge circuit and one of the signal lines, and a low-impedance across the pre-charge circuit.

2. The system of claim 1, where the pre-charge circuit comprises a resistor located between one of the contacts and the device.

3. The system of claim 1, comprising a switch located between the contacts and the device.

4. The system of claim 3, where the switch is a field effect transistor located between the contacts and the device.

5. The system of claim 3, where the switch is configured to conduct after the low-impedance is provided across the pre-charge circuit.

6. The system of claim 1, comprising reference contacts configured to provide a common reference to the bus and the device before contact between the pre-charge circuit and one of the signal lines as the device is inserted onto the bus.

7. The system of claim 1, comprising power contacts and reference contacts, where the reference contacts are configured to provide a common reference to the bus and the device before the power contacts provide power, and the power contacts provide power before contact between the pre-charge circuit and one of the signal lines as the device is inserted onto the bus.

8. (Cancelled).

9. The system of claim 1, comprising power contacts, where the power contacts are configured to provide power at the same time as contact between the pre-charge circuit and one of the signal lines, as the device is inserted onto the bus.

10. The system of claim 1, where the signal lines comprise a serial data line and a serial clock line.

11. The system of claim 1, where the bus is an inter-integrated circuit bus.

12-30. (Cancelled).

31. A system, comprising:

a bus comprising signal lines;

a device configured to be inserted onto and removed from the bus through contacts configured to provide at different times during insertion and removal contact between a pre-charge circuit and one of the signal lines, and a low-impedance across the pre-charge circuit,

the contacts comprising a connector system including a first connector, a second connector, where the first connector is configured to provide a first pre-charge circuit between the second connector and a first bus signal line, and the second connector is configured to provide a first short-circuit between the second connector and the first bus signal line, where the first connector and the second connector are staggered to provide the first pre-charge circuit and the first short-circuit at different times during engagement and disengagement of the connector system.

32. The system of claim 31, comprising:

a third connector; and

a fourth connector, where the third connector is configured to provide a second pre-charge circuit between the fourth connector and a second bus signal line, and the fourth connector is configured to provide a second short-circuit between the fourth connector and the second bus signal line, where the third connector and the fourth connector are staggered to provide the second pre-charge circuit and the second short-circuit at different times during engagement and disengagement of the connector system.

33. The system of claim 32, where the first connector and the third connector are staggered to simultaneously provide the first pre-charge circuit between the second connector and the first bus signal line and the second pre-charge circuit between the fourth connector and the second bus signal line.

34. The system of claim 32, where the first connector and the third connector are staggered to provide the first pre-charge circuit between the second connector and the first bus signal line and the second pre-charge circuit between the fourth connector and the second bus signal line in a sequence.

35. The system of claim 32, where the second connector and the fourth connector are staggered to simultaneously provide the first short-circuit between the second connector and the first bus signal line, and the second short-circuit between the fourth connector and the second bus signal line.

36. The system of claim 32, where the second connector and the fourth connector are staggered to provide the first short-circuit between the second connector and the first bus signal line, and the second short-circuit between the fourth connector and the second bus signal line in a sequence.

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.